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. 100

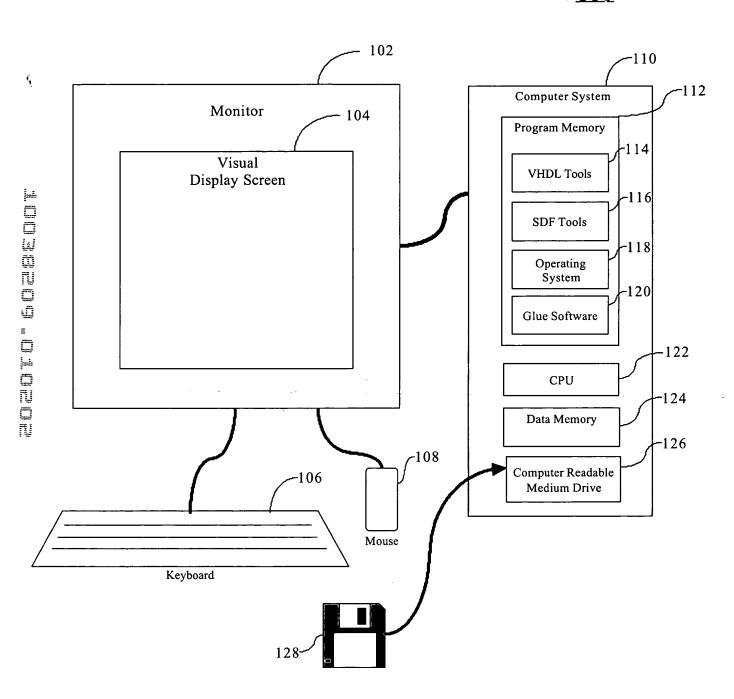


FIG 1

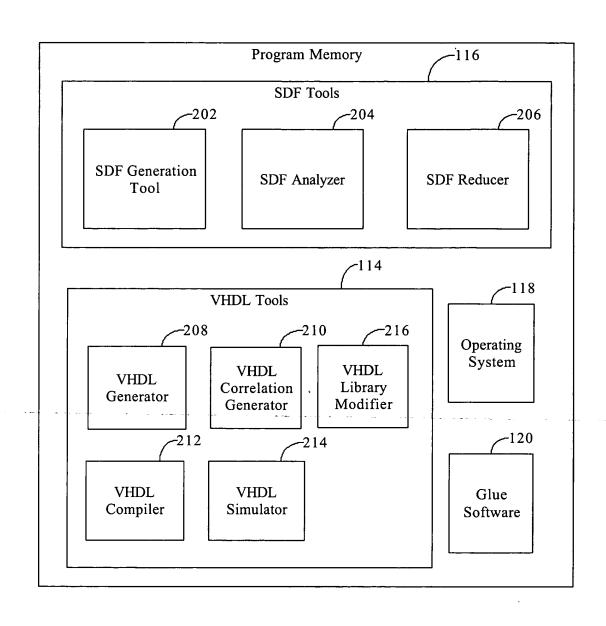


FIG 2

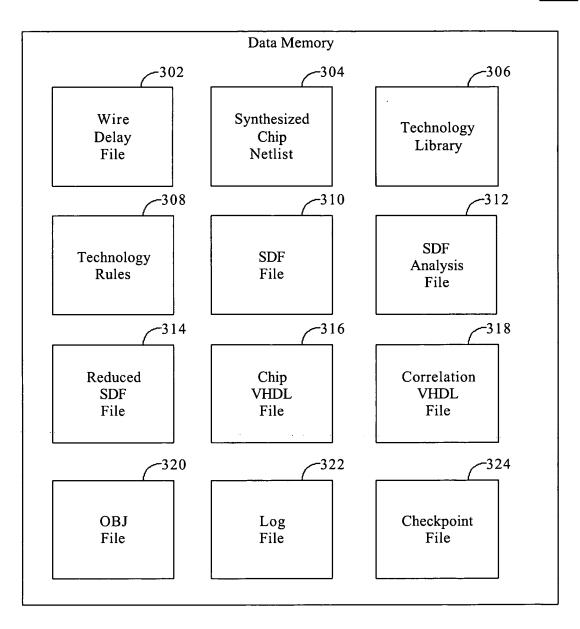
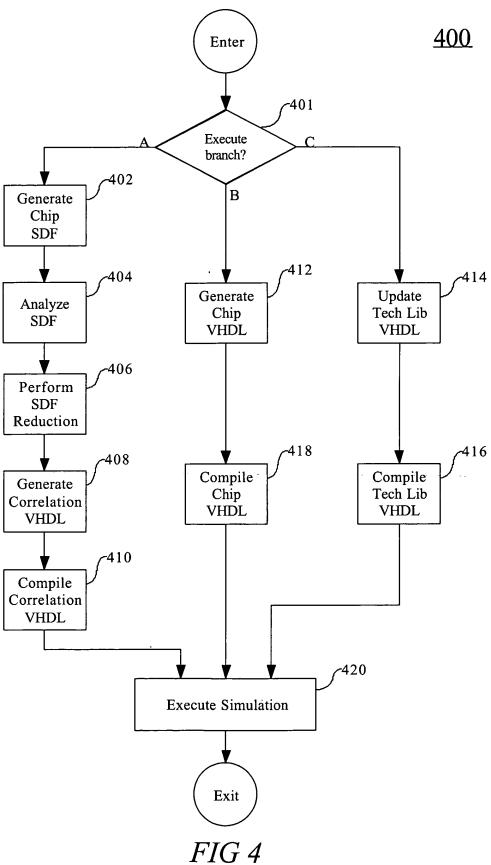


FIG 3

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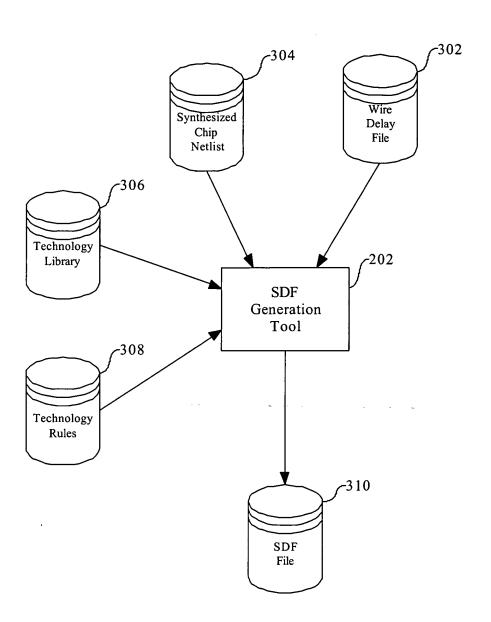


FIG 5

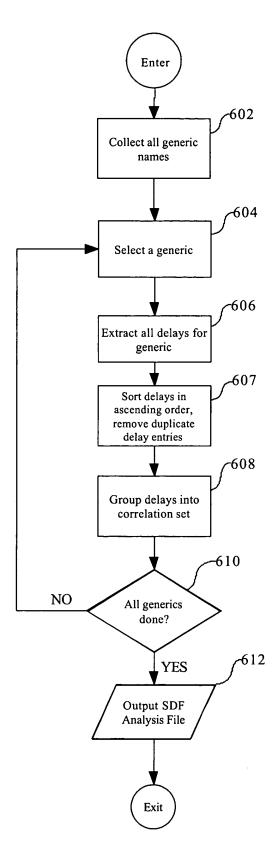


FIG 6



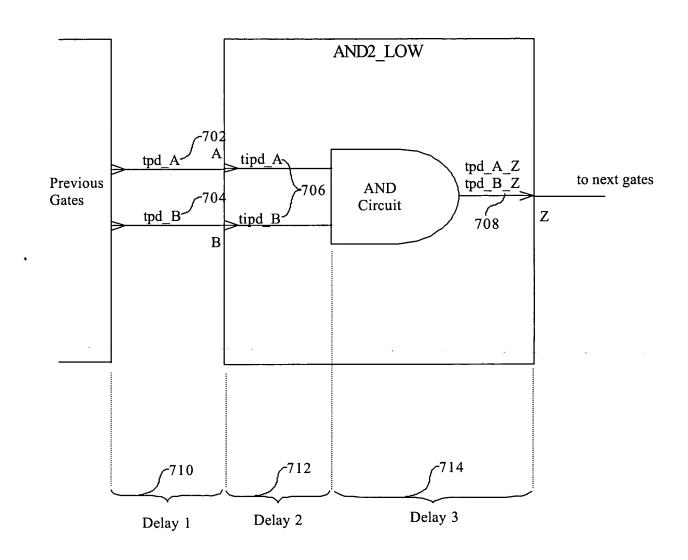


FIG 7

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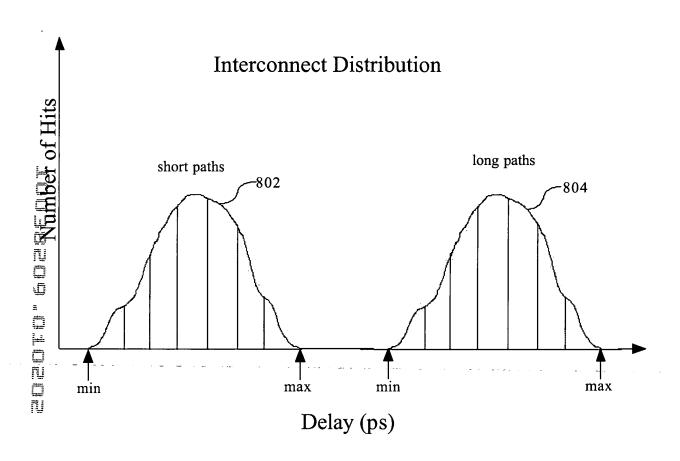


FIG 8

<u>900</u>

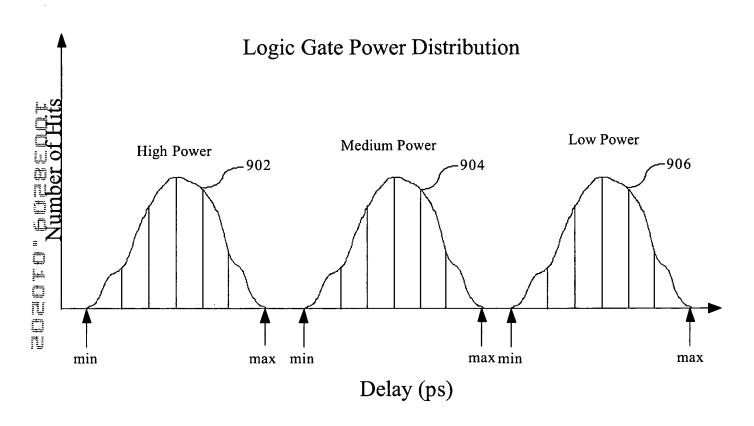


FIG 9

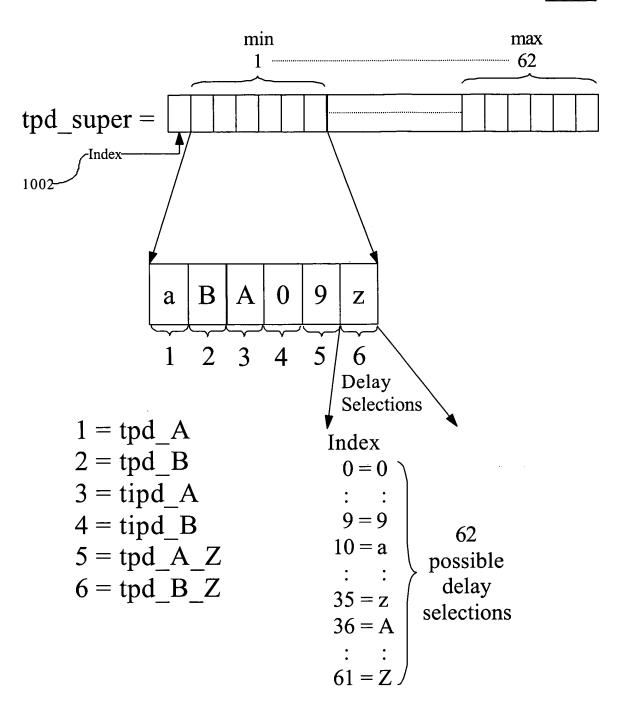


FIG 10

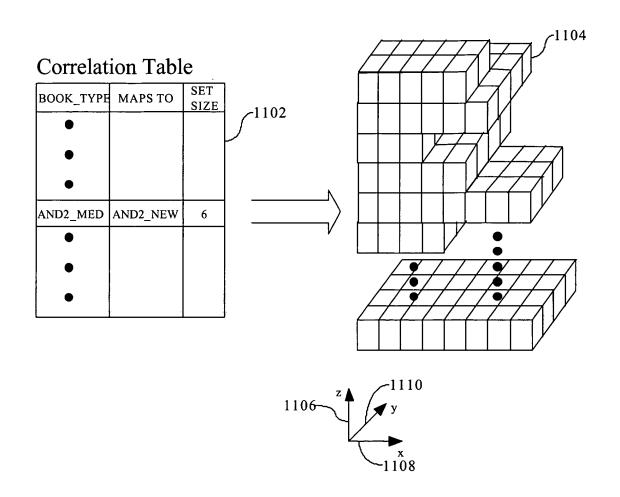
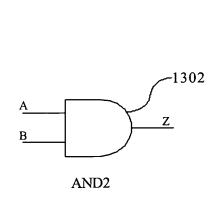


FIG 11

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CHAR POSITION (0 OFFSET)	VALUE	Correlation Set (x')	Entry Position (y')	Slot Offset (x")
0	1	N/A	N/A	N/A
1	4	1	5th	1st
2	X	1	60th	2nd
3	а	1	11th	3rd
4	m	1	26th	4th
5	р	1	29th	5th
6		1	25th	6th

FIG 12



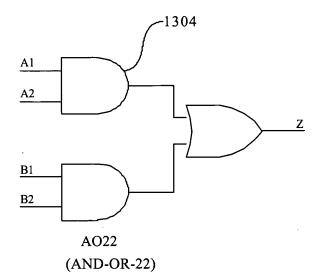


FIG 13

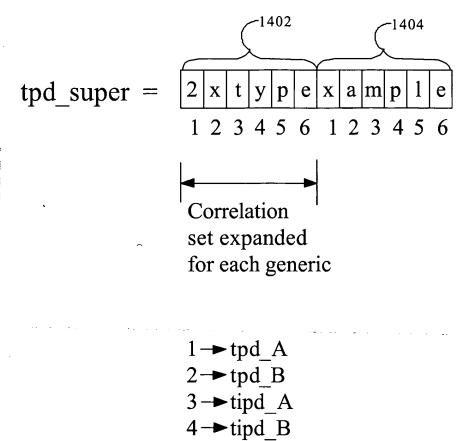


FIG 14

 $5 \rightarrow \text{tpd}_A Z$  $6 \rightarrow \text{tpd}_B Z$ 

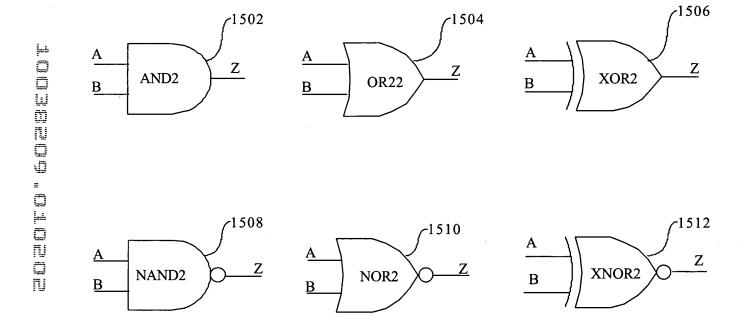
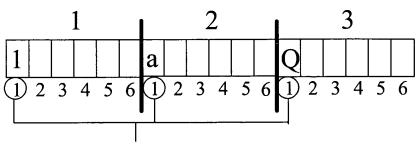


FIG 15

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# 1600



tpd\_A positions for AND2 gate

### Encode as:

DELAY		tpd_A		
	DELAY	1	2	3
	-0.500 ns	0	0	0
	-0.499 ns	0	0	11
٦	•	•	•	는 • 七
_	•		• •	
	+237.826 ns	Z	Z	Υ
	+237.827 ns	Z	Z	Z

FIG 16

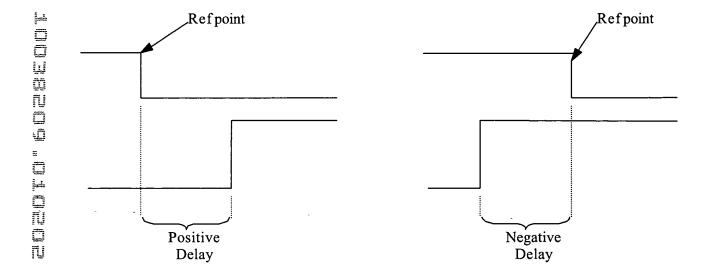


FIG 17



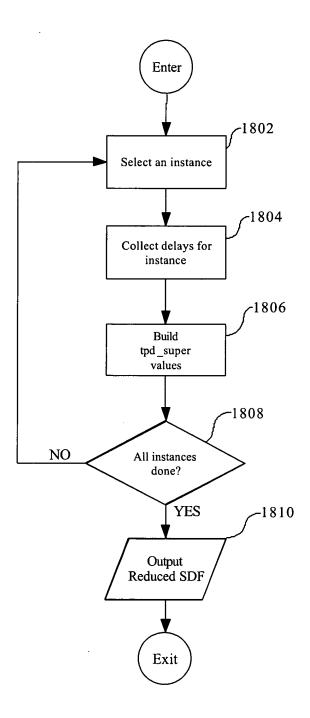


FIG 18

### <u>408</u>

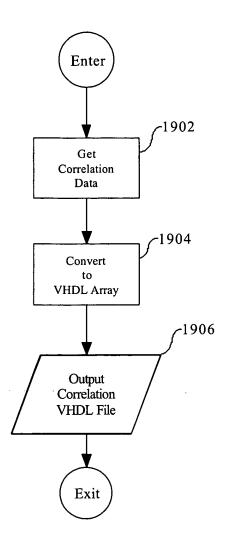


FIG 19

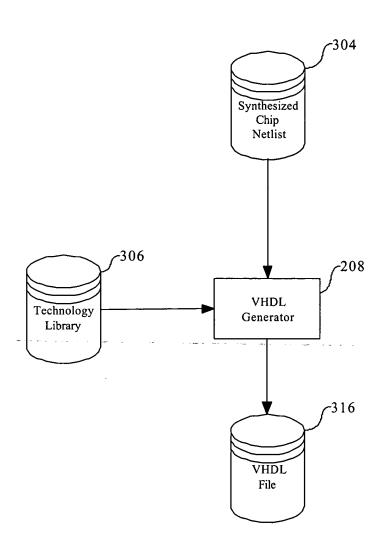


FIG 20

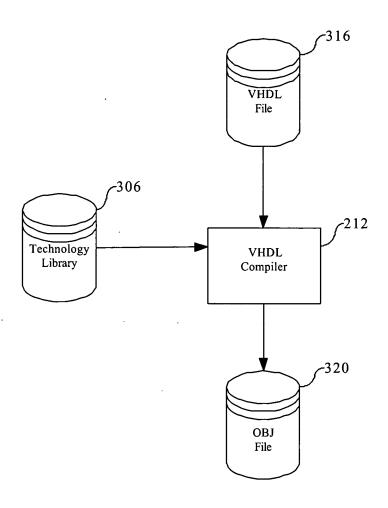


FIG 21

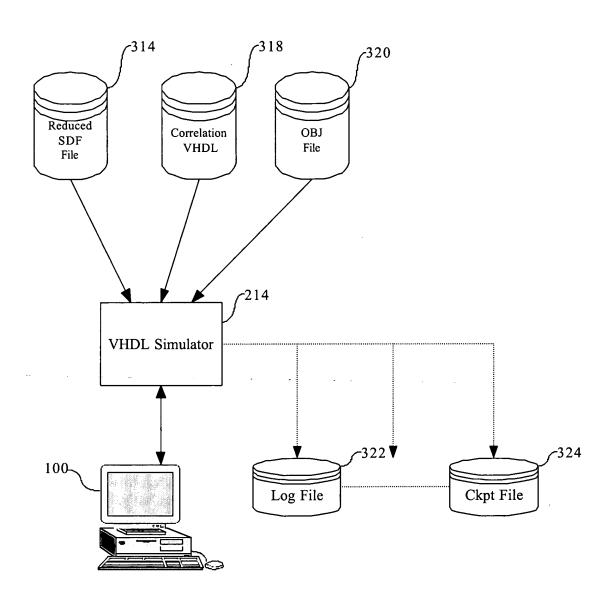


FIG 22